What is claimed is:

1. A test circuit comprising:

an input circuit inputting data to select a test mode relative to a circuit to be tested and outputting result of selection of the test mode in synchronization with a first clock;

a pattern generation circuit, responding to result of selection of the test mode, generating a test pattern in synchronization with a second clock and outputting the test pattern to a circuit to be tested;

a comparator inputting result of test of the circuit to be tested in synchronization with the second clock, and comparing coincidence/non-coincidence between the result of the test and the test pattern supplied to the circuit to be tested; and

an output circuit holding result of comparison by the comparator means and outputting the result of comparison in synchronization with the first clock.

2. The test circuit according to claim 1 wherein

the comparator compares the result of test and the test pattern so as to detect a defect part of the circuit to be tested; and

the output circuit holds result of detection by the comparator and outputs the result of detection in synchronization with the first clock.

3. A test circuit comprising:

an input circuit inputting data to select a test mode relative to a circuit to be tested and outputting result of selection of the test mode in synchronization with a first clock;

a pattern generator responding to result of selection of the test mode, generating a test pattern in synchronization with a second clock and outputting the test pattern to a circuit to be tested, and outputting a test pattern end signal representing end of generation of the test pattern;

a comparator inputting result of test of the circuit to be tested in synchronization with the second clock, and comparing coincidence/non-coincidence between the result of the test and the test pattern supplied to the circuit to be tested; and

an output circuit holding result of comparison by the comparator means and outputting the result of comparison in synchronization with the first clock.

4. The test circuit according to claim 3, wherein

the comparator means compares the result of test and the test pattern so as to detect a defect part of the circuit to be tested; and

the output means holds result of detection by the comparator and outputs the result of detection in synchronization with the first clock.

5. A semiconductor memory comprising:

an input circuit inputting data to select a test mode relative to a circuit to

be tested and outputting result of selection of the test mode in synchronization with a first clock;

a pattern generation circuit, responding to result of selection of the test mode, generating a test pattern in synchronization with a second clock and outputting the test pattern to a circuit to be tested;

a comparator inputting result of test of the circuit to be tested in synchronization with the second clock, and comparing coincidence/non-coincidence between the result of the test and the test pattern supplied to the circuit to be tested;

an output circuit holding result of comparison by the comparator means and outputting the result of comparison in synchronization with the first clock

a logic circuit for executing a logical operation in synchronization with the first clock being formed on the same semiconductor circuit; and

a clock generator generating the second clock so as to supply the second clock to the test circuit being provided inside or an outside of the semiconductor substrate.